AMENDMENTS TO THE CLAIMS

Please amend claim 6 to read as follow:

1. (Previously Presented) A thin film transistor comprising:

a buffer layer formed on a substrate;

an activation layer formed on said buffer layer; and

a gate insulation layer formed on said substrate including said activation layer,

with said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer, and said step being a half or less of the thickness sum of said activation layer and gate insulation layer,

said buffer layer has a step to such a degree that thickness of said gate insulation layer is not changed on said side wall of said buffer layer.

Claims 2-4. (Cancelled)

5. (Previously Presented) The thin film transistor according to claim 1, wherein said activation layer being a polysilicon, and a thickness of the gate insulation layer is 400 Å or more when a thickness of said polysilicon is 300 Å and step is 350 Å in said activation layer.

6. (Currently Amended) The thin film transistor according to claim 1, wherein said activation layer being [[an]] polysilicon, and thickness of the gate insulation layer is 1,000 Å or more when a

thickness of said polysilicon is 500 Å and said step is 750 Å in said activation layer.

7. (Original) A method for fabricating said thin film transistor of claim 1, comprising the steps of:

depositing an amorphous silicon layer on a substrate equipped with buffer layer;

forming a polycrystalline silicon layer by crystallizing said amorphous silicon layer;

forming an activation layer by etching said polycrystalline silicon layer;

treating the surface of said activation layer; and

depositing a gate insulation layer on said substrate,

with etching time being controlled in said activation layer forming process and activation layer surface treatment process so that step between a lower part of gate in the buffer layer and a part except the lower part of said gate has a step value corresponding to a half or less of the thickness sum of said activation layer and gate insulation layer.

8. (Original) The method for fabricating a thin film transistor according to claim 7, wherein the etching time is controlled so that said buffer layer has a step to such a degree that thickness of said gate insulation layer is not changed on said side wall of said buffer layer.

9. (Original) The method for fabricating a thin film transistor according to claim 7, wherein the etching time is controlled to accommodate said buffer layer having a step corresponding to a half or less of the thickness sum of the activation layer and gate insulation layer.

10. (Original) The method for fabricating a thin film transistor according to claim 9, wherein the etching time is controlled so that said buffer layer has a step to such a degree that thickness of said gate insulation layer is not changed on said side wall of said buffer layer.

11. (Original) The method for fabricating a thin film transistor according to claim 7, wherein a thickness of said gate insulation layer is 400 Å or more when the thickness of solid-phase crystallization polysilicon is 300 Å and step is 350 Å in said activation layer.

12. (Original) The method for fabricating a thin film transistor according to claim 7, wherein thickness of said gate insulation layer is 1,000 Å or more when the thickness of excimer laser annealing polysilicon is 500 Å and step is 750 Å in said activation layer.

13. (Previously Presented) A thin film transistor, comprising:

a buffer layer;

an activation layer formed on said buffer layer; and

a gate insulation layer formed on said buffer layer and said activation layer,

with said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer, and said step being up to a half of the thickness sum of said activation layer and gate insulation layer,

said step being controlled according to said gate insulation layer being deposited to an even

thickness on a side wall of said activation layer.

Claim 14. (Cancelled)

15. (Previously Presented) The thin film transistor according to claim 13, with said activation layer comprising a polysilicon, and a thickness of said gate insulation layer being at least 400 Å when a thickness of said polysilicon is 300 Å and step is 350 Å in said activation layer.

16. (Previously Presented) The thin film transistor according to claim 13, with said activation layer comprising a polysilicon, and a thickness of said gate insulation layer being at least 1,000 Å when a thickness of said polysilicon is 500 Å and step is 750 Å in said activation layer.

Claims 17-20. (Cancelled)

21. (Previously Presented) The thin film transistor according to claim 1, wherein a thickness of the gate insulation layer is at least 400 Å when a thickness of said activation layer is 300 Å and step is 350 Å in said activation layer.

22. (Previously Presented) The thin film transistor according to claim 1, wherein the step of said buffer layer being formed on a single body of said buffer layer with the step protruding from a flat portion of said buffer layer.